Explanation of Amendments in the Claims:

1.(currently amended) Apparatus for direct digital generation of a synthesized RF signal with phase modulation at a desired output frequency comprising:

a high speed reference clock providing in an input signal having a series of signal reference edges at a frequency of the reference clock which is higher than the desired output frequency;

programmable digital delay elements arranged to receive the reference edges of the input reference clock and to generate delayed signal edges each at a calculated delay from a respective reference edge;

wherein the programmable digital delay elements include an input element for receiving an increment value ~~data~~ defining the ~~a~~ required phase modulation and providing a delay value for said calculated delay from said increment value;

wherein the programmable digital delay elements comprises a high speed adders/accumulator which is arranged to determine the amount of delay implemented by the delay elements on the reference edge;

and wherein the output frequency is set from the increment value according to the following equation:

Increment Value = $((f_{ref} / f_{out}) -1) * 2^n$

where f_{ref} = Reference clock frequency

f_{out} = Output frequency

n = Number of bits in the accumulator math;

and a signal combining element for receiving the delayed signal edges and for generating the RF signal therefrom.

2.(cancelled)

3.(currently amended) The apparatus according to Claim 1 wherein the programmable digital delay elements comprise ~~high speed adders/accumulators and~~ a look-up table for providing increments to be added to calculate said delay.

4.(original) The apparatus according to Claim 3 wherein the lookup table has a multiple set of lookup tables to be used for temperature compensation of the programmable delay line.

5.(original) The apparatus according to Claim 1 wherein the reference clock provides an external input with high frequency absolute accuracy and very low phase noise performance.

6.(original) The apparatus according to Claim 1 wherein the programmable digital delay elements are arranged such that said reference edge may be either the rising or falling edge of the reference clock.

7.(original) The apparatus according to Claim 1 wherein said programmable digital delay elements have separate controls for producing the rising and falling edges of the output from the same input edge of the reference clock.

8.(currently amended) The apparatus according to Claim 1 wherein the programmable digital delay elements are arranged to be varied by altering the input ~~clock~~ signal of the reference clock.

9.(currently amended) The apparatus according to Claim 1 ~~2~~ wherein in association with the high speed adder/accumulator ~~adders/accumulators of the programmable delay elements~~ there is provided a pulse swallow circuit which is controlled by the carry bits (overflow bits) of the high speed adder/accumulator ~~adders/accumulators~~ in order to extend the delay to multi cycles of the ~~input~~ reference clock.

10.(currently amended) The apparatus according to Claim 9 wherein the pulse swallow circuit is arranged to discard multiple ~~reference clock~~ pulses of the reference clock.

11.(original) The apparatus according to Claim 9 wherein said pulse swallow circuit is located prior to or following the high speed adder/accumulator ~~programmable delay element~~.

12.(original) The apparatus according to Claim 1 wherein the high speed adder/accumulator ~~programmable digital delay element~~ are arranged such that 360 degrees of phase delay of the programmable delay is calibrated to 2^n of the phase accumulator value using a look up table or microprocessor.

13.(currently amended) The apparatus according to Claim 1 ~~wherein the programmable digital delay elements comprise high speed adders/accumulators wherein said adders/accumulators are arranged to determine the amount of delay implemented by the delay elements on the reference edge and~~ wherein the input element comprises a modulation adder for providing a value to be added to the delay from said accumulator/adders.

14. The apparatus according to Claim 13 wherein said

modulation adder is ~~adders are~~ arranged to add in ~~the~~ positive or negative phase offset to the accumulator value to produce the required phase modulation.

15.(currently amended) The apparatus according to Claim 13 wherein there is provided an interpolator which is arranged to interpolate ~~the~~ sampled base band modulated information to provide ~~said~~ data for said modulation adder.

16.(original) The apparatus according to Claim 15 wherein the interpolator is a linear interpolator or a sin x/x interpolator filter.

17.(currently amended) The apparatus according to Claim 15 wherein the interpolator is arranged such that the need for a reconstruction filter is removed by interpolation up to the input signal ~~reference clock~~ rate of the reference clock.

18.(currently amended) The apparatus according to Claim 15 wherein there is provided a plurality of separate interpolators for both ~~the~~ rising and falling pulse edges of the reference clock.

19.(original) The apparatus according to Claim 1 wherein the signal combining element comprises a flipflop.

20.(currently amended) The apparatus according to Claim 19 wherein said flipflop is arranged to combine the delayed signal edges from separate rising and falling pulse edges of the reference clock ~~edge delays~~ to form any desired duty cycle output.

21.(currently amended) The apparatus according to Claim 20 wherein said output duty cycle is not dependent on an input duty cycle of the

input signal of the reference clock.

22.(currently amended) The apparatus according to Claim 1 ~~20~~ wherein an ~~said~~ output duty cycle is ~~of the output can be~~ varied relative to an input duty cycle by changing a ~~the~~ difference in initialization values of ~~the~~ two separate adders/accumulators forming the programmable digital delay elements for the separate rising and falling pulse edges of the reference clock ~~edge delay control~~.

23.(cancelled)

24.(currently amended) The apparatus according to Claim 22 wherein the output duty cycle is set by initializing a ~~the~~ difference of the initializing values of the two separate adders/accumulators according to the following equation:

The difference equals the reference clock frequency divided by the desired output frequency multiplied by $2^{\wedge n}$ multiplied by (p/100), where p is the percentage duty cycle and n is the number of bits in the accumulator math.

25.(cancelled)

26.(currently amended) The apparatus according to Claim 1 ~~2~~ wherein the number of bits of math used in the adder/acumulator is ~~can be~~ equal to or exceeds the number of bits of control in lookup table and /or the programmable delay.

27.(currently amended) The apparatus according to Claim 1 wherein the speed is ~~can be~~ increased by using parallel processing in the high speed adder/accumulator ~~adders, and/or accumulators~~.

28.(currently amended) The apparatus according to Claim 1 ~~2~~ wherein the adder/accumulator ~~adders/accumulators~~ is implemented in a larger lookup table wherein all the table ~~answers of the pattern are~~ precomputed and stored.

29.(original) The apparatus according to Claim 1 wherein the components are formed fully digitally in an ASIC with no requirement for a voltage controlled oscillator, loop filter, or Digital to Analog converter.

30.(original) The apparatus according to Claim 1 wherein there is further provided amplification and filtering of the output to produce a signal that is higher in amplitude and/or having less harmonics.